Q3 Known Good Substrates Technical Report
CONTRACT/PR NO. N00014-07-C-0918 Dow Corning Corporation
Quarterly Technical Report
Reporting Period: 1 March 2008 – 31 May 2008

Executive Summary

At the end of the third program quarter defect levels are tracking at or near program goals, yet some metrics have deteriorated from their best values during the program. Process alterations are being tested to drop MPD<10/cm2 and improve doping uniformity and defect count in epitaxy, the results of these efforts will be reported in Q4. All subcontractors have epiwafer materials. Device fabrication is in process at NGES and Microsemi. Two lots of PiN devices are complete at GeneSiC and device testing is initiated.

Technical Progress

The following table documents the key program end metric goals.

Metric	50th Percentile	20th Percentile
MPD distribution 4H n+ 76 mm diameter (cm^{-2})	10	5
MPD distribution 4H n+ 100 mm diameter (cm^{-2})	20	10
Net scratch length by LLS relative to wafer diameter (%)	40	20
Equivalent Epitaxy Defect Density 76 mm diameter (cm^{-2})	<10	<5
Epitaxy Doping Target Accuracy	+/- 25%	+/-10%
Epitaxy Doping Variation within wafer (Max-Min/Min, %)	35%	10%
Substrate Resistivity Maximum 4H n+ 76mm	0.025	0.020

Progress Against Metrics

The following charts show early progress against the program metrics. Due to extended processing cycles, data tends to become available 4-6 weeks in the rears.

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14. ABSTRACT
The Known Good Substrates (KGS) Phase II program was initiated 29 August 2007. Wafer, epitaxy, modeling and metrology work has been the main focus of efforts in Q3. This technical report summarizes the progress by all team members against the tasks and milestones.

15. SUBJECT TERMS
SiC wafer, SiC epitaxy, SiC material metrology

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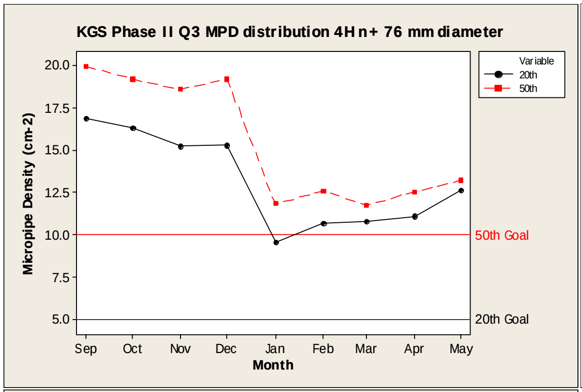

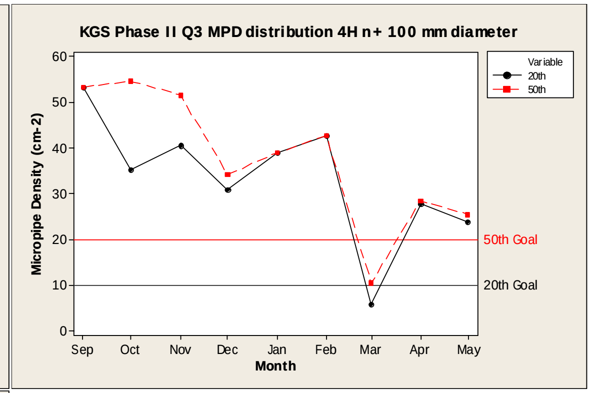

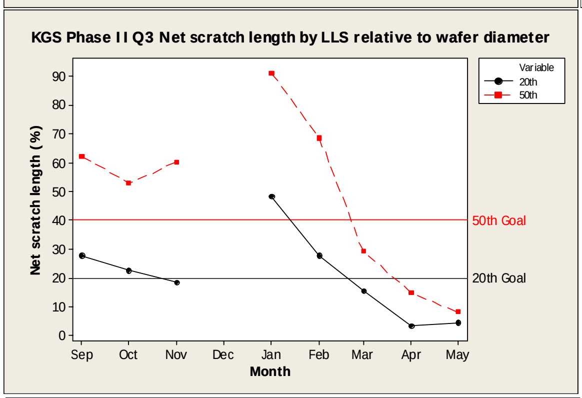

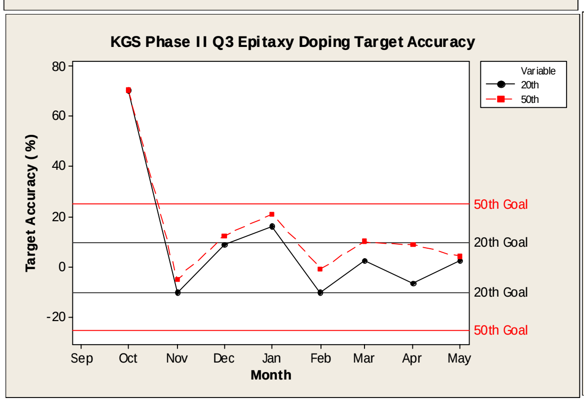

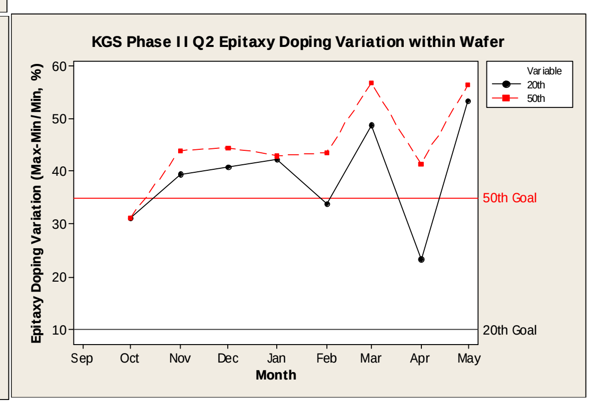

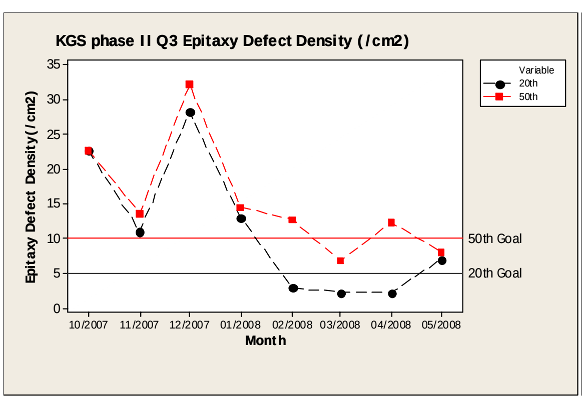

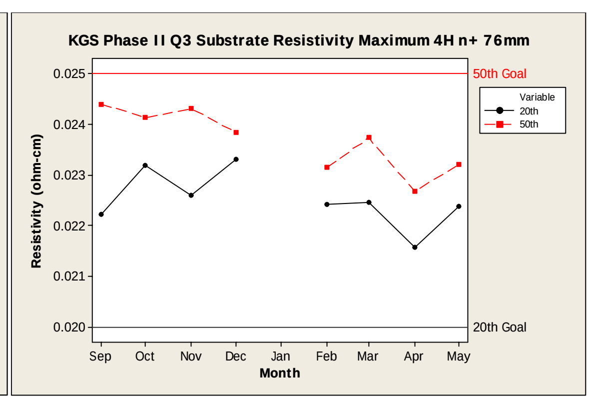

Details by task follow:

Task 1: SiC Wafers Products

Highlights:

- Studies of the resistivity variations within a n+ 4H SiC crystal have identified methods to reduce both the absolute resistivity level and the variation within the crystal. DCCSS has now started a program to gradually reduce the resistivity in 4H n+ SiC towards the program targets.
- Studies of the defect formation processes in wafer polishing have identified a route to reduce scratches on the surface. The methods were tested in Q3. The results show dramatically lower net scratch length per wafer as measured by LLS meeting both the 50^{th} and 20^{th} percentile goals of the program. Wafers are now processed with scratch lengths typically less then 10% of the wafer diameter.
- Greater then 40 Epitaxial wafers have been manufactured to specification and shipped to contract partners, including MicroSemi, Northrop Grumman, NRL, and ASU, for device fabrication and testing. This completes the wafer deliverables to MicroSemi for the program.

Roadblocks: (Red text are roadblocks from previous report)

- Highly N_2 doped 4H SiC materials manufactured to meet the 20^{th} percentile resistivity goal continue to have low crystal yields due to cracking during ingot fabrication. Resistivity reduction now achievable, see highlights.
- Scratch defects are above goal. Rework of polished parts from Q1 has successfully reduced scratches (new Q1 values are below what was presented in the last report). Defects significantly improved, see highlights
- Excessive epitaxial related defects in the first part of Q2 limited the ability to produce epitaxial wafers for subcontractors. However improvements in Q2 have greatly reduced this problem. Improvements in Q2 appear to be holding in Q3.
- Epitaxial doping uniformity continues to be a challenge with uniformity values tracking higher then the 50^{th} percentile goal. Work has started to reduce the doping uniformity by investigating process chemistry via modeling.

Task 2: Continuous Improvements in SiC Substrates

Highlights

- Growth process modifications have provided a mechanism to shift median boule resistivity from 0.024 to 0.021 Ω-cm for the within wafer maximum. Initial results suggest this improvement can occur without any degradation in process yields. A roadmap is being implemented to gradually reduce resistivity to program targets.
- Process modifications have improved crystal yield for 100mm materials by 2-3X relative to Q1 of the program and have resulted in micropipe densities for 100mm close to the 50^{th} percentile goal.

- Improvements in the epitaxial growth process have reduced the epitaxy defect density in Q3 of the program. This has allowed for epitaxial wafer with high device yields (predicted by LLS) to be produced and sent to contract partners for device fabrication.
- An improved growth furnace RF heat source has been demonstrated by modeling to improve growth variability. The improved growth furnace RF heat source will be implemented into a PVT furnace for testing in Q4.
- Modeling work and crystal growth nucleation studies continue to help improve the efficacy of DCCSS's new PVT growth technology. Several trials show MPD with values near or below 10/cm2 and much improved lattice curvature. The method will be tested at a higher throughput in Q4.

Roadblocks

- Tracking towards the 76mm MPD 20th percentile goal has slowed in Q3. Micropipe reduction to <5 cm-2 needs to be accelerated, which is being addressed with crystal growth modeling and growth initiation studies.
- Micropipe targets for 100mm still not at project targets. High micropipe densities at the edge of the crystals due to persistent grain boundaries are limiting micropipe reduction.
- Target values for in-wafer resistivity still not achieved. Project goals are being addressed through continued growth process modifications and alteration of source technology to encourage impurity incorporation

Task 3: Metrology for Wafer Specifications.

Highlights

- New wafer polish technology to reduce scratch defects has required modification of device killer defect signatures in LLS tests. The recipe of LLS yield prediction for bare wafer has been modified. Yield prediction from new recipe show very good agreement with both the defect density and map from KOH etch analysis.
- Epitaxy defect map has been developed to characterize origin of failures on each device die. Spatial distribution of epitaxy added defects show no correlation with wafer position in the batch epitaxy growth and distribution of wafer micropipes.
- Small embedded particles, which are dominant epitaxy added defects and have been reduced greatly with the new epitaxy process in Q2. Now epitaxy defects show rounded surface morphology and are embedded tightly in epitaxy layer, as compared to epitaxy pits showing typically material towers with very well defined facets before the end of Q2. Studies will now focus to find the source of the new defects.

Task 4: Device Technology Maturation

Highlights

MOS and SBD characterization

- Generation lifetime - Generation lifetimes are limited by the $EH_{6/7}$ center in 4H-SiC. Recent published results suggest that recombination lifetime is dominated by $Z_{1/2}$ defect. Thus, generation and recombination lifetimes in 4H-SiC are determined by different defects. In the case of extremely short generation lifetimes which are often accompanied by a strong electric field dependence, dislocations can interact with other impurities and become "decorated" which can change generation lifetime greatly. The effect of the cut-off angle of the substrate on generation lifetime shows no significant difference between 4 and 8 degree wafers. The correlation of generation lifetime with etch pits indicates that the generation lifetime is not directly limited by etch pit densities in the range of mid 10^4 cm^{-2}. Generation lifetimes, however, show good correlation with birefringence images to have the lowest lifetime in the sample which has many defect features. This can be related with a threshold dislocation density and generation lifetime is limited by dislocations when dislocation density is above it.
- Recombination lifetime of PiN wafers - It is clear that measured recombination lifetime values decrease significantly in the presence of the p+/n- interface relative to that measured on wafers with n- drift layer alone. Lifetimes from interrupted and continuous p+/n- growth show no significant lifetime difference between two methods. The results show the lifetime reduction with p+ layer can be related with high recombination rate at the interface of p+ and n- layers.
- SBD characterization – In-grown stacking faults and discrete threading edge dislocations revealed by EBIC technique do not degrade Schottky barrier height (SBH) and ideality factor. Impacts of scratches from polishing and carrots from epitaxy growth to SBH are not clear at the moment.

Roadblocks

- Majority of wafer shipments to major device contractors (Microsemi, GeneSiC, NGES) were completed in late Q2/Early Q3. The delays in shipping wafers have put the program about 10 weeks behind schedule. Subcontractors now have epiwafers to complete contract work. First device results are expected in early Q4.

Progress toward Milestones for End of Program (Sub-bullets are progress this quarter)

- Correlation Maps of PiN forward IV characteristics and recombination lifetime
    - first two lots now in testing.
- Correlation of PiN forward IV characteristics and n+ epitaxial buffer layer/MP blocking
    - first two lots now in testing
- Primary SiC material defect limiting PiN performance (Roadmap input - GeneSiC)
- SiC materials parameter assessed as most important for SIT performance improvements based on wafer probe data (Roadmap input - NGES)
    - First lots are now in device fabrication.
- SiC materials parameter assessed as most important for SBD performance improvements based on wafer probe data (Roadmap input - Microsemi)
    - SBD lots in device fabrication at Microsemi.

- Generational improvement of 4H SiC wafer crystal quality summarized by XRT and MPD analysis
    - XRT analysis is showing improvement in crystal quality, MPD has dropped close to goal but is now stalling. Analysis of several new crystals from an altered PVT process will be available in July.
- Assessment of oxide quality for 76mm/100mm 4H epiwafers and link to generation lifetime
    - Wafers still in test at NRL and ASU.

Schedule

Program device fabrication work is still at 8 weeks behind schedule.

Program Management

No activity this quarter.

Appendix 1: KGS Subcontractors and Quarterly Progress Points

Subcontractor	Area of Focus	Progress This Quarter
Northrup Grumman Electronics Systems	J-SIT fabrication and testing	Epiwafers delivered in early March. More work in Q4 expected at DCCSS in order to improve uniformity of doping for use in future trials.
Microsemi	SBD fabrication and testing	All epiwafers delivered, includes comparisons of old and improved epitaxy process (defect control), old and new wafer polish method and substrates from next generation PVT process. Two lots of SBD in process, initial probe of first devices shows good forward bias characteristics.
GeneSiC Semiconductors	PiN diode fabrication and testing	First two lots of PiN diode wafers have been fabricated. Next 3 lots have entered device fab.
SUNY – Stoney Brook	Crystal Structure of SiC	Work has focused to understand the effect of scratches on forming defects in the epitaxy layer. It has been found that the orientation of the scratch

		with respect the crystal axes will most influence how defects propagate into the epitaxial layer.
Arizona State University	SiC Oxides, carrier lifetime and device failure analysis	Generation lifetime analysis. Oxidation induced defect generation study and charge burst tests. (Dr. Schroder) 6 epi wafer delivered for SBD and PiN diodes. Preliminary data from the thermal imaging. PL imaging for stacking faults. (Dr. Skromme)
Fluxtrol	Modeling and design of high uniformity induction heating systems	New RF heating arrangement is to be delivered in Q4.
NRL	SiC Oxides, Epitaxy, Lifetime testing, materials testing, device testing	3 bare wafers and 13 epi wafers delivered for various devices. UV-PL image of a bare wafer from KGS II shows much less defect signatures as compared to the wafer from KGS I.
STR	Modeling of CVD and PVT SiC Growth Processes	Now focusing efforts on CVD epitaxy chemistry. Initial models show that the distribution of reactants above the wafer for both Si and C are much different than expected, and inspire ideas as to improving doping uniformity.

<u>Publications</u>

Submitted to ECSCRM 2008

1. Carrier Generation Lifetimes in 4H-SiC Epitaxial Wafers

Gil Chung**,** M.J. Loboda, M.J. Marninella, D.K. Schroder, T. Isaacs-Smith and J.R. Williams

2. Wafer Level Recombination carrier lifetime measurements of 4H-SiC PiN Epitaxial Wafers

Gil Chung, M.J. Loboda, M.F. MacMillan, and J.W. Wan